

MX368041A

W-CDMA Software

(For MG3681A Digital Modulation Signal Generator)



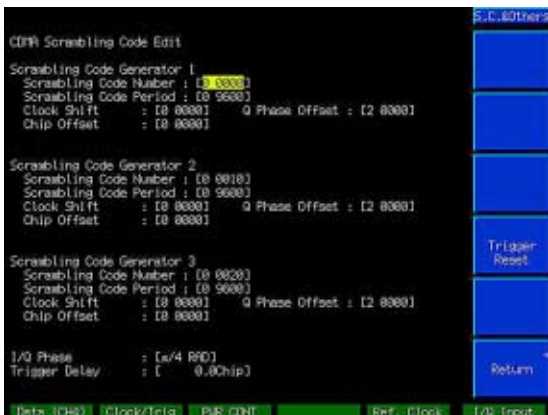
For Evaluating Third Generation Mobile Communications System

3GPP standard W-CDMA Modulation Signals Outputs

The MX368041A W-CDMA Software is installed in the MU368040A CDMA Modulation Unit, when the MU368040A is housed in the MG3681A Digital Modulation Signal Generator. It can output uplink and downlink of W-CDMA modulation signals for 3GPP (FDD) standard.

Connection with User Equipment and Base Station

This function can generate P-CCPCH, P-SCH, S-SCH, and CPICH for synchronizing the user equipment (UE) simultaneously to the equivalent of three base stations. In addition, an external trigger function for controlling the CDMA modulation signal timing is useful in the base station test.



Scrambling code editing

Supports 3GPP Test Specifications

Pattern data based on the 3GPP test specifications, such as base station test models standardized in TS25.141 and downlink multiplex signals with OCNS for maximum input level test standardized in TS25.101, are included in the software. These pattern data can perform modulation based on the test specifications.



Pattern data check window

Multiplex Signals Generation

The signal up to 12 channels can be multiplexed for any settable channel such as the channelization code and code power, etc. And multiplex signals can be added up to 512 channels (at Phase 1).



Main screen

Modulation Data Download Function

The special test pattern and specification updates are supported by the pattern data downloaded from PC memory card.

Power Control Function

An external control signal can control the channel power in 1-slot steps. In addition, the code power on each channel can be programmed up to a 64-slot cycle. This is useful for checking the power control operation.

Supports Chip Rates up to 16.5 Mcps

The CDMA modulation signal in the 3GPP specifications can be set chip rates of 1.6 to 16.5 Mcps in 1 cps steps.

Variable Baseband Filter Function

In addition to setting the baseband filter to Nyquist or Root Nyquist, the roll-off ratio can be set from 0.10 to 1.00 in 0.01 steps.

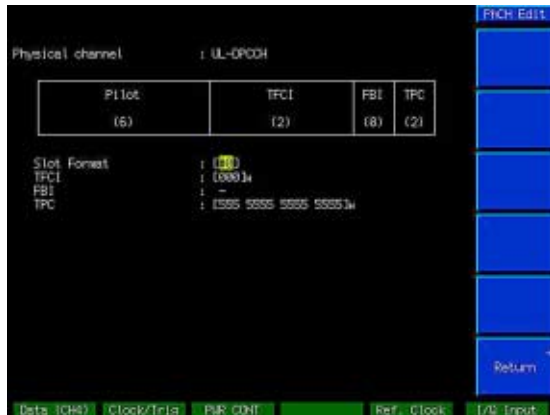
Real Time Generation of Modulation Signals in Each Format

Five physical channels and two transport channels can be selected on the screen.

And the each parameter for these channels can be edited and modulation signals can be generated based on various test specifications.

User Equipment Simulation

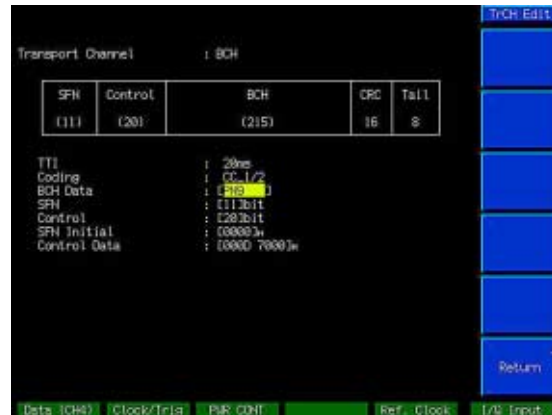
The DPCCCH and DPDCH physical channel formats can be selected. In addition to being able to edit the TFCI and slot format for DPCCCH, the TPC bit can be edited in a 60-slot cycle.



DPCCCH editing

BCH Editing Function

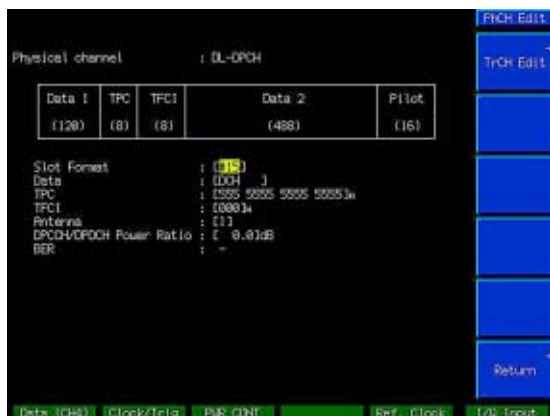
BCH can be selected in the P-CCPCH data at downlink and be edited. The BCH editing screen is used to edit the SFN bit count, SFN initial, control bit count, etc.



BCH editing

Base Station Simulation

The P-CCPCH, CPICH, DL-DPCH physical channel format can be selected. It is possible to set the open loop Tx diversity (TSTD, STTD) on or off in each channel. In addition to being able to edit the TFCI and slot format for DPCH, the TPC bit can be edited in a 60-slot cycle.



DL-DPCH editing

DCH Editing Function

DCH can be selected in the DL-DPCH data at downlink and the DPDCH data at uplink and be edited. The DCH editing screen is used to edit the transport channel count, rate matching attribute, etc. This supports reference measurement channel 12.2/64/144/384 kbps and BTDF specified by 3GPP TS25.101/104, AMR and ISDN specified by 3GPP TR25.944 etc. It is also possible to insert BER and BLER up to 10% in 0.1% steps.

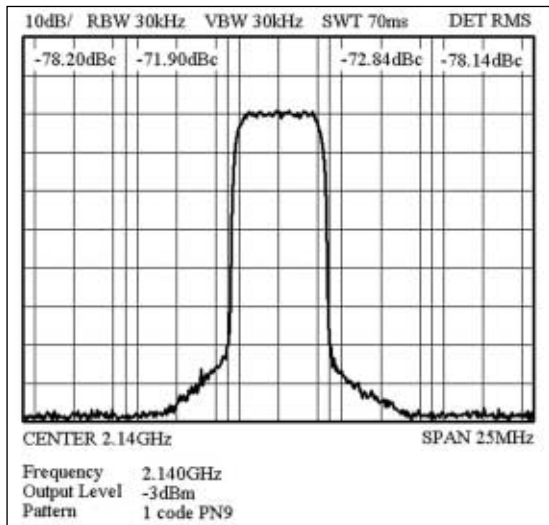


DCH editing

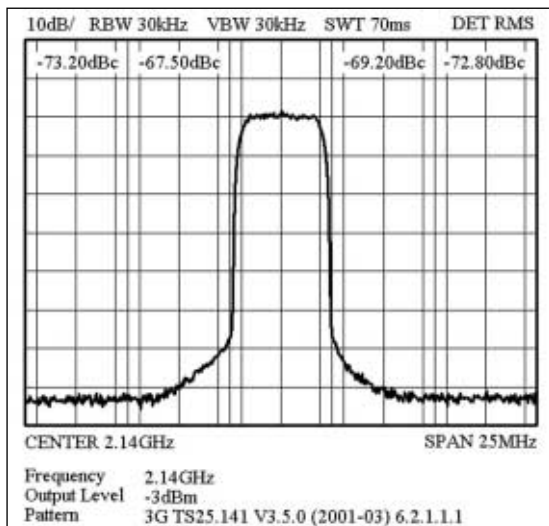
Excellent Analog Performance/Various Options

Adjacent Channel Leakage Power Ratio

The adjacent channel leakage power ratio of the digital modulation signal generator is an important factor in distortion testing of device and interference testing of receivers. The MG3681A achieves an excellent adjacent channel leakage power ratio by an optimized circuit design. The typical adjacent channel leakage power ratio for W-CDMA system is -68 dBc/3.84 MHz and the secondary adjacent channel leakage power ratio is -75 dBc/3.84 MHz.



Adjacent channel leakage power ratio at 1 code signal



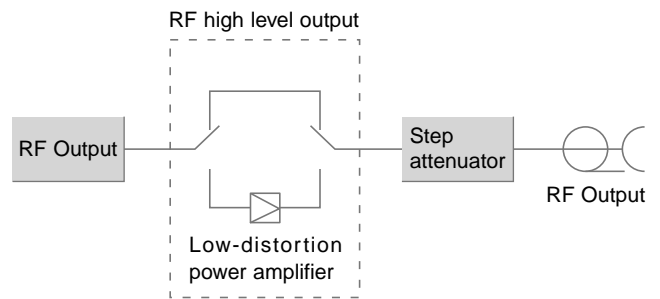
Adjacent channel leakage power ratio at 16 code multiplex

AWGN Supports Dynamic Range Test

When performing the receiver dynamic range test specified by 3GPP, AWGN with the W-CDMA modulation signal is required. When the MU368060A AWGN Unit is installed in the MG3681A, a high-precision AWGN can be output in the 4 to 16 MHz bandwidth. Moreover, since one MG3681A can output a signal that is the internally added W-CDMA uplink modulation signal and the AWGN, is useful for simple test of the base station receiver dynamic range.

RF Level-up at Modulation

When the RF high level output (Option 42) is installed in the MG3681A, the RF level can be output 8 dB gain without degrading the adjacent channel leakage power ratio in the W-CDMA system frequency band (1.9 to 2.3 GHz). This is very useful for signal source of power amplifier requiring a high input level.



RF high level output option installation diagram

Eliminate to Out-Band Spurious

When outputting a W-CDMA signal at the MG3681A, measurement may sometimes be interfered with by spurious* that is generated due to the circuit composition. In such a case, unwanted signals can be eliminated by connecting the MA2512A Band Pass Filter to the RF output of the MG3681A. The MA2512A has excellent amplitude and group delay characteristics in the W-CDMA system frequency band (1.92 to 2.17 GHz), so it does not degrade the MG3681A modulation accuracy.

*: 660 MHz, output frequency + 660 MHz, 2nd/3rd harmonics



MA2512A Band Pass Filter

Specifications

This software is installed in the MU368040A.

Supported systems	W-CDMA (FDD)
Spreading method	Direct spread
Modulation method	Uplink: BPSK (data), HPSK (spreading) Downlink: QPSK (data), QPSK (spreading)
Supported phase	Phase 1, 2, 3 (Phase 2 and 3 only support chip rate)
Number of multiplex channel	Phase 1: 1 to 512, Phase 2: 1 to 1024, Phase 3: 1 to 2048
Spreading factor	Phase 1: 1 to 512, Phase 2: 1 to 1024, Phase 3: 1 to 2048
Chip rate	Phase 1: 1.6 to 4.125 Mcps, Phase 2: 3.2 to 8.25 Mcps, Phase 3: 6.4 to 16.5 Mcps
Symbol rate	Chip rate/Spreading factor
Transfer rate accuracy	MG3680 series main frame reference signal accuracy; external reference signal accuracy at external sync
Filter mode	ACP (adjacent channel leakage power priority), EVM (vector accuracy priority)
Baseband filter	Nyquist/Root Nyquist, roll-off ratio: 0.1 to 1.0 (0.01 steps)
Number of arbitrary setting code	1 to 12 (post-spread processing setting)
Download data	Number of symbol data channel: Max. 2 channels (number of channel able to download physical layer data at coding from outside; max. 9 codes at multi code) Symbol data length: 4M symbols/channel (no power sequence), 1M symbols/channel (with power sequence) Waveform data length Any waveform data: 512 Kwords x 2 channels (1 word = 16 bits)
Internally generate channel format	Base station simulation
	<p>P-CCPCH (& SCH) Data: PN9, PN15, PN9 fix, 16 bit repeat, BCH TSTD: On/off STTD: 1, 2 [Data = at BCH selection] SFN: Select as 0 to 16 bits (settable initial value) Control: Select as 0 to 32 bits (input 32 bit data) Data: PN9, PN15, PN9 fix, 16 bit repeat</p> <p>CPICH Antenna: 1, 2</p> <p>DL-DPCH Slot format: Depends on set spreading factor Data: PN9, PN15, PN9 fix, 16 bit repeat, DCH TPC: 4 frame cyclic pattern TFCI: 0 to 3FFh Antenna: 1, 2 DPCCH/DPDCH power ratio BER: 0% to 10% (0.1% resolution) [Data = at DCH selection] Transport channels: 1 to 8 DTX: fix, flexible Data: PN9, PN15, PN9 fix, 16 bit repeat TTI: 10, 20, 40 ms TrBk Size: Depends on encoder and Tr channel count CRC: 0, 8, 12, 16, 24 bits Coder: No coding, convolution (coding rate: 1/2, 1/3), turbo (coding rate: 1/3) Rate matching attribute: 100 to 300 BER: 0% to 10% (0.1% resolution) BLER: 0% to 10% (0.1% resolution)</p>

Internally generate channel format	User equipment simulation	<p>DPCCH Slot format: Depends on spreading factor setting TPC: 4 frame cyclic pattern TFCl: 0 to 3FFh FBI: 4 frame or 2 frame cyclic pattern</p> <p>DPDCH Slot format: Depends on spreading factor setting Data: PN9, PN15, PN9 fix, 16 bit repeat, DCH TPC: 4-frame cyclic pattern TFCl: 0 to 3FFh [Data = at DCH selection] Transport channel: 1 to 8 Data: PN9, PN15, PN9 fix, 16 bit repeat TTI: 10, 20, 40 ms TrBk Size: Depends on encoder and Tr channel count CRC: 0, 8, 12, 16, 24 bit Coder: No coding, convolution (coding rate: 1/2, 1/3), turbo (Coding rate: 1/3) Rate matching attribute: 100 to 300 BER: 0% to 10% (0.1% resolution) BLER: 0% to 10% (0.1% resolution)</p>
	Base station simulation	<p>Channelization code: Any setting for each code Encoding: OVSF Setting range (channelization code No.): 0 to (spreading factor -1) Scrambling code*1 Code: M sequence gold Scrambling code No. setting: 00000h to 3FFFFh Scrambling code default phase setting: 00000h to 3FFFFh Scrambling code Q-phase offset setting: 00000h to 3FFFFh Scrambling code cycle setting: 00001h to 40000h</p>
Spreading signal	User equipment simulation	<p>Channelization code: Any setting for each code Encoding: OVSF Setting range (channelization code No.): 0 to (spreading factor -1) Scrambling code*1 Encoding: M sequence gold (HPSK,QPSK selectable) Scrambling code No. setting: 0000000h to 1FFFFFFh Scrambling code cycle setting: 0000001h to 2000000h</p>
Internally generated data (without coding)		Pseudo-random pattern (PN9, 15, 23) or any 16 bit repeat (CH11, 12 are max. 32 bit variable cyclic pattern)
Code power setting		-40 to 0 dB, off, 0.1 dB resolution
Power control		Internal program function: Slot power of each channel programmable in 2 to 64 slot cycle (1 dB resolution) External control function: Any code power controllable at external signal (TTL level) synchronized with slot (1 dB resolution)
Offset		Settable frame offset for scrambling code (1 symbol resolution) Settable offset between each scrambling code (1 chip resolution)
I/Q phase		I/Q output symbol point selection: 0, $\pi/4$ rad
External signal	Input signal	<p>Data: Physical layer (before spread processing) serial data input Frame clock/trigger: External frame sync signal input (adjustable trigger delay) Power control: External power control signal input (any 1 code 1 dB step power control) Reference clock: Chip rate 2^n time baseband sync signal input (n: Phase 1 = 0 to 2, Phase 2 = 0 to 1, Phase 3 = 0) Input connector: TTL Level, BNC connector (front panel)</p>
	Output signal	<p>Data clock: Data sync clock output Data: Symbol data output before diffusion Symbol clock: Symbol clock output synchronized to data Reference clock: Chip rate 2^n times clock output (n: Phase 1 = 0 to 3, Phase 2 = 0 to 2, Phase 3 = 0 to 1) Frame clock: Wireless frame cycle pulse output Slot clock: Time slot cycle pulse output Code: Channelization code and scrambling code exclusive OR Output connector: TTL level, BNC connector (rear panel)</p>
I/Q signal	Output level	$\sqrt{I^2 + Q^2} = 0.200$ V (rms) *Number of max. multiplex: at 1 signal, filter mode: EVM, 50 Ω termination, BNC connector (front panel)
	Vector accuracy	$\leq 3\%$ (rms) *Chip rate: 3.84 Mcps, number of max. multiplex: 1 signal, filter mode: EVM, 18° to 35°C

RF signal	Frequency range	10 to 3000 MHz
	Output level range	-143 to +5 dBm (number of max. multiplex: at 1 to 7 signals) -143 to +4 dBm (number of max. multiplex: at 8 to 12 signals) -143 to +3 dBm (number of max. multiplex: at 13 to 15 signals) -143 to +2.14 dBm (number of max. multiplex: at 16 to 19 signals) -143 to +2 dBm (number of max. multiplex: at 20 to 31 signals) -143 to +1 dBm (number of max. multiplex: at 32 to 50 signals) -143 to 0 dBm (number of max. multiplex: at ≥ 51 signals)
	Continuous mode variable range	-10 to +8 dB (number of max. multiplex: excluding at 16 to 19 signals) -10 to +7.14 dB (number of max. multiplex: at 16 to 19 signals)
	Burst on/off ratio	>60 dB (1.9 to 2.3 GHz)
	Vector accuracy	$\leq 2\%$ (rms) *1.9 to 2.3 GHz, 0 dBm, chip rate: 3.84 Mcps, number of max. multiplex: 1 signal, filter mode: EVM
	Carrier leak	≤ -30 dBc (≤ 0 dBm, 18° to 35°C, 1.9 to 2.3 GHz)
	Image rejection	≤ -40 dBc (≤ 0 dBm, after calibration, 1.9 to 2.3 GHz)
	Level accuracy	Level accuracy: ± 1.2 dB compared with CW level (1.9 to 2.3 GHz, chip rate: 3.84 Mcps, number of max. multiplex: 1 signal, scrambling code: on, power control function: off)
	Adjacent channel leakage power ratio	-64 dBc/3.84 MHz (5 MHz offset), -71 dBc/3.84 MHz (10 MHz offset) -68 dBc/3.84 MHz (typ. 5 MHz offset), -75 dBc/3.84 MHz (typ. 10 MHz offset) *1.9 to 2.3 GHz, -3 dBm, number of max. multiplex: 1 code signal, filter mode: ACP, 18° to 35°C, spectrum analyzer method, RMS detection
	Spurious	< -60 dBc (1.9 to 2.3 GHz, chip rate: 3.84 Mcps, number of max. multiplex: 1 signal, filter mode: ACP)
Firmware backup space	CDMA: 300 KB, DSP: 250 KB, FPGA: 100 KB	

*1: With 3 generators, select each channel and settable to off. Each generator start timing can be set with a resolution of 1 chip.

Ordering Information

Please specify the model/order number, name, and quantity when ordering.

Model/Order No.	Name	Remarks
MG3681A*1	Main frame Digital Modulation Signal Generator	250 kHz to 3000 MHz
MG3681A-42	Option RF high level output	1.9 to 2.3 GHz, 8 dB gain
MU368040A*1 MU368060A*1	Expansion Units CDMA Modulation Unit AWGN Modulation Unit	
MX368041A W1759AW	Software W-CDMA Software Standard accessories MX368041A operation manual: 1 copy	With CompactFlash card (with adapter) or ATA flash memory card
MA2512A*1	Application parts Band Pass Filter	1920 to 2170 MHz

*1: Refer to the separate catalogs for the MG3681A, MU368040A, MU368060A, and MA2512A.

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Specifications are subject to change without notice.

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